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APPLICANT:

Mikko Waltari

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**U.S. PATENT DOCUMENTS**

Examiner Initials	Cite No.	Document Number	Publication Date/ Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code			
<i>JPW</i>	AA	5,212,486	05-18-1993	Nagaraj <i>341/172</i>	
	AB	5,510,789	04-23-1996	Lee <i>341/120</i>	
	AC	5,644,308	07-01-1997	Kerth et al. <i>341/120</i>	
	AD	5,861,832	01-19-1999	Nagaraj <i>341/161</i>	
	AE	US 6,535,157B1	03-18-2003	Garrity et al. <i>341/163</i>	

**FOREIGN PATENT DOCUMENTS**

Examiner Initials	Cite No.	Foreign Patent Document	Publication Date/Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>1</sup>

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>1</sup>
<i>JPW</i>	AF	KRISHNASWAMI NAGARAJ, Senior Member; Efficient Circuit Configurations for Algorithmic Analog to Digital Converters; IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing; December 1993; pp. 1-9; Vol. 40, No. 12	

EXAMINER:

*Robert W. Wang*

DATE CONSIDERED:

*04/07/2005*

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